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EXAMINER	
PATEL, ASHOKKUMAR B	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 07/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,487	TU ET AL.	
	Examiner	Art Unit	
	Ashok B. Patel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are subject to examination.

Response to Arguments

2. Applicant's arguments filed May 03, 2005 have been fully considered but they are not persuasive for the following reasons:

Claim 1:

35 U.S.C. §103(a) Rejections:

Applicant's argument:

Applicant respectfully submits that while arbitration to identify a first modification request may be resolved on a round-robin basis. the Examiner has not shown any obvious combination to arrive at allowing the first modification request to succeed if the identified ownership state corresponds to the first requesting device, which is precisely what the Examiner has admitted was not disclosed by the cited reference.

Examiner's response:

First of all, Examiner would like to respectfully request the Applicant to refer to Simcore et al. (US 5, 418, 967), col. 1 through col. 2, line 60 for examples of known arbitration systems including round-robin and priority.

Second, what Examiners had admitted in the previous Office Action is again reiterated here, "Although, the reference Derrick teaches that the first modification request is allowed to succeed if the identified ownership state corresponds to no ownership, and indicates that Bus controller (Arbiter) assigns a priority which determines which semaphore modification request is allowed, the reference fails to

explicitly teach to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device, however it is well known in the art to implement the desired protocol for the priority determining the order of granting the requests for semaphore modifications such as round robin."

As clearly pointed out by Derrick in col. 4, line 35-38, that "Bus controller 402 controls accesses by bus masters 406 to shared resources 408, allowing only one bus master 406 to have control or ownership of any given shared resource 408 at any given time.", and in the same column, line 43-45, Derrick goes on elucidating that " Bus controller 402 may control accesses by bus masters 406 to shared resources 408 using any suitable scheme."

As such, there has to exist "any suitable scheme" in order for Derrick's Bus controller (arbiter) to control access by bus masters (requesting devices) for, as Derrick has stated, "allowing only one bus master 406 to have control or ownership of any given shared resource 408 at any given time." Therefore, Examiner had admitted "the reference fails to explicitly teach to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device" wherein Derrick had failed to specifically point out "any suitable scheme" that will allow its Bus Controller to "allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device."

Applicant's argument:

"Derrick's device simply locks out accesses by other requesting devices to the same semaphore without knowing if it is owned by another master. It is the requesting

device of Derrick. rather than a machine to receive the requests, that checks to see if the shared resource is owned by another device (Fig. 2, steps 204. and 206. col. 3, lines 57-64)."

"In Claim 1, a machine that receives the semaphore modification requests identifies an ownership state of the semaphore and allows the first modification request to succeed if the identified ownership state corresponds to the first requesting device. Since that one machine accesses the semaphore to identify the ownership state, exclusive access to a semaphore is guaranteed and the locks of Derrick are not required."

"Examiner states that. *'whether a lock or locks of Derrick is/are required must not be viewed as any differentiating element.'* Applicant respectfully intends that the relevant differentiating elements set forth by Claim 1 are identifying an ownership state of a semaphore. arbitrating to identify a first modification request from a first requesting device and allowing the first modification request to succeed if the identified ownership state corresponds to the first requesting device." And "Such differentiating elements as set forth by Claim I are clearly not disclosed or suggested by the cite references, as the Examiner has admitted."

Examiner's response:

First of all, Derrick clearly discloses in col. 4, line 35-38, that "Bus controller 402 controls accesses by bus masters 406 to shared resources 408, allowing only one bus master 406 to have control or ownership of any given shared resource 408 at any given time." , and in the same column, line 43-45, Derrick goes on elucidating that " Bus

controller 402 may control accesses by bus masters 406 to shared resources 408 using any suitable scheme." Therefore, it is the machine that identifies the request in order to control access using any suitable scheme.

The previous Office Action does indicate as, "whether a lock or locks of Derrick is/are required must not be viewed as any differentiating element as part of the reference's teaching in establishing the relevancy, direct or indirect, since there is no concrete mention made; indicated, stated, or described, about the "lock or locks" in the claim."

The differentiating elements set forth by Claim 1 are relevant to Derrick's teachings of "any suitable scheme" by which "Bus controller 402 may control accesses by bus masters 406 to shared resources 408 (Derrick, col. 4, line 43-45)" and "Note that spin buffer 520 has the flexibility to discriminate between individual bus masters (e.g., 406A-406D), or in the alternative, may simply discriminate based on the port on which the device is connected. , (col.5, line 61 through col.6, line 9) since claim 1 clearly recites "arbitrate to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device;" and therefore the differentiating elements set forth by Claim 1 are not relevant to "lock or locks" as there is no concrete mention made; indicated, stated, or described, about the "lock or locks" in claim 1."

Also, for responses to Applicant's arguments regarding claims 17, 8, 14 and 24, please refer to the above. In addition, please also note that Derrick teaches the spin buffer where the lock and identification data within the semaphore is cached in a multiprocessor environment. (Abstract). Semaphore memory holds the semaphore for the entire set of resources (Fig.6, element 504). Spin buffer is a semaphore checker (Fig.6, element 502, spin buffer) that is coupled to arbiter is a resource scheduling device and the semaphore (Fig.6, element 504, semaphore memory). The arbiter is a resource scheduling device that is coupled to the logical plurality of processing devices (Fig.6, element 506). Spin buffer thus provides the information within the semaphore relating to the ownership status of the shared resource. (col.3, lines 3-5).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Derrick et al. (hereinafter Derrick) (US 5,872,980) in view of Dao et al. (hereinafter Dao) (US 6,148,395).

Referring to claims 1, 2, 3, 6 and 7,

1. A article of manufacture including one or more machine-accessible medium having executable code stored thereon which, when executed by a machine, causes the machine to:

receive one or more semaphore modification requests from one or more requesting devices;

identify an ownership state of a semaphore corresponding to the one or more semaphore modification requests;

arbitrate to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device;

allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device; and

allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

2. The article of manufacture recited in Claim 1 which, when executed by a machine, further causes the machine to:

decline a second modification request of the one or more semaphore modification requests.

3. The article of manufacture recited in Claim 1 which, when executed by a machine, further causes the machine to:

receive a semaphore read requests from one of the one or more requesting devices;

transmit the identified ownership state in response to the semaphore read request; and

allow the first requesting device to access a shared resource.

6. The article of manufacture recited in Claim 1 wherein arbitration is resolved on a round-robin basis.

7. The article of manufacture recited in Claim 1 wherein arbitration is resolved on a priority basis.

Derrick teaches the spin buffer where the lock and identification data within the semaphore is cached in a multiprocessor environment. (Abstract). Spin buffer thus provides the information within the semaphore relating to the ownership status of the shared resource. (col.3, lines 3-5). When the devices (fig.5, Bus Masters, 406A, 406B, 406C, and 406D) need access to a shared resource and after they initiate the read for the ownership (requests for semaphore modification), spin buffer detects (receives) the read for ownership from the devices. Spin buffer then identifies the ownership state of a semaphore corresponding to the requests (col. 5, lines 34-39). If the semaphore is owned by another device , the requesting device is denied access to the shared resource (declining second modification request). If the requested semaphore is not owned by another requesting device, then the requesting device can read the data from the semaphore which completes the process of acquiring the ownership of the shared resource (transmitting the identified ownership state and allow the first requesting device to access a shared resource) (col.4, lines 3-9) . Bus controller along with Spin

buffer also provides arbiter which determines whose and when to allow the request for resource ownership to succeed based on the priority and availability of a shared resource (Fig. 4, element 402 (Bus Controller), Fig.5, element 506 (Arbiter), col.4, lines 43-56). Although, the reference Derrick teaches that the first modification request is allowed to succeed if the identified ownership state corresponds to no ownership, and indicates that Bus controller (Arbiter) assigns a priority which determines which semaphore modification request is allowed, the reference fails to explicitly teach to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device, however it is well known in the art to implement the desired protocol for the priority determining the order of granting the requests for semaphore modifications such as round robin. Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a means which causes machine to receive the requests for semaphore modifications, to identify an ownership state of a semaphores corresponding to semaphore modification requests, arbitrate and allow the modification requests to succeed as desired, in this case the first modification request to succeed if the identified ownership state corresponds to the first requesting device. Because, it is economical and efficient to share a resource among multiple processors rather than each processor is having a complete set of resources.

Referring to claims 4 and 5,

4. The article of manufacture recited in Claim 1 wherein the semaphore is stored in a multiprocessor comprising the one or more requesting devices.

5. The article of manufacture recited in Claim 4 wherein the multiprocessor comprising the one or more requesting devices is integrated on a single die.

Keeping in mind the teachings of Derrick as indicated above, Derrick does not teach storing the semaphore in a multiprocessor and multiprocessor comprising the one or more requesting devices integrated on a single chip. Dao teaches the semaphore stored in a multiprocessor and the multiprocessor comprising the one or more requesting devices integrated on a single chip in the environment offering shared resources like floating point unit and cache. The multiprocessor also includes the logic control including arbitration for the use of certain shared resources and for updating status information regarding the current state of the device.(Abstract, Fig.1, col. 3, lines 34-43, col. 11, lines 20-25). Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to integrate the spin buffer, arbiter, and semaphore memory of Derrick for storing the semaphore in a multiprocessor where multiprocessor comprises of one or more CPUs (requesting devices) on a single die as taught by Dao. Because, as inferred by the teaching of Dao, when requesting devices are integrated on a single chip, the chip size is reduced which translates into high manufacturing yield and low per-chip manufacturing cost.

Referring to claims 8, 9,10, 12 and 13,

8. A method comprising:

receiving one or more semaphore modification requests from one or more requesting devices;

identifying an ownership state of a semaphore corresponding to the one or more semaphore modification requests;

arbitrating to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device;

allowing the first modification request to succeed if the identified ownership state corresponds to the first requesting device; and

allowing the first modification request to succeed if the identified ownership state corresponds to no ownership

9. The method recited in Claim 8 further comprising declining a second modification request of the one or more semaphore modification requests.

10.The method recited in Claim 8 further comprising:

receiving a semaphore read requests from one of the one or more requesting devices;

transmitting the identified ownership state in response to the semaphore read request; and

allowing the first requesting device to access a shared resource.

12. The method recited in Claim 8 wherein arbitration is resolved on a round robin basis.

13. The method recited in Claim 8 wherein arbitration is resolved on a priority basis.

Claims 8, 9, 10, 12 and 13 are the methods associated with the article of manufacture of claims 1,2,3,6 and 7. Therefore claims 8, 9, 10, 12 and 13 are rejected for the reasons set forth in above paragraph for claims 1, 2, 3, 6 and 7.

Referring to claim 11,

11. The method recited in Claim 8 wherein each of the one or more semaphore modification requests received identify a corresponding requesting device of the one or more requesting devices.

Derrick teaches having a separate identification of each requesting devices connected to each port of spin buffer thus Derrick's spin buffer is capable of discriminating between the individual devices when it comes to prioritizing the semaphore modification requests. (col.5, lines 53-67 and col.6, lines 1-9).

Referring to claims 14 and 15,

14. A multiprocessor system comprising:

means for receiving one or more semaphore modification requests from one or more requesting devices;

means for identifying an ownership state of a semaphore corresponding to the one or more semaphore modification requests;

means for arbitrating .to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device;

means for granting the first modification request if the identified ownership state corresponds to the first requesting device; and

means for granting the first modification request if the identified ownership state corresponds to no owner.

15. The multiprocessor system recited in Claim 14 further comprising:

means for receiving a semaphore read requests from one of the one or more requesting devices;

means for transmitting the identified ownership state in response to the semaphore read request; and

means for allowing the first requesting device to access a shared resource.

Claims 14 and 15 include a multiprocessor system that implement the methods of claims 8 and 10 associated with the article of manufacture of claims 1 and 3. Therefore claims 14 and 15 are rejected for the reasons set forth in above paragraph for claims 1, 2, 3, 6 and 7.

Referring to claim 16,

16. The multiprocessor system recited in Claim 14 wherein the one or more requesting devices are fabricated on a single die.

Claim 16 is rejected for the reasons set forth in above paragraph for claims 4 and 5.

Referring to claim 17,18, 19, 22 and 23,

17.A multiprocessor comprising:

a logical plurality of processors;

a resource scheduling device coupled to one or more of the logical plurality of processors to provide access to a set of resources;

a shared resource of the set of resources having a semaphore;

a semaphore checker coupled to the resource scheduling device and to the semaphore to:

receive one or more semaphore modification requests from the one or more of the logical plurality of processors,

identify an ownership state of the semaphore,

arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting processor of the one or more of the logical plurality of processors,

allow the first modification request to succeed if the identified ownership state corresponds to the first requesting processor; and

allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

18. The multiprocessor recited in Claim 17 wherein the semaphore checker is further to:

decline a second modification request of the one or more semaphore modification requests.

19. The multiprocessor recited in Claim 17 wherein the semaphore checker is further to:

receive a semaphore read requests from one of the one or more of the logical plurality of processors;

transmit the identified ownership state in response to the semaphore read6 request; and

allow the first requesting processor to access a shared resource.

22. The multiprocessor recited in Claim 17 wherein arbitration is resolved on a round-robin basis.

23. The multiprocessor recited in Claim 17 wherein arbitration is resolved on a priority basis.

Derrick teaches the spin buffer where the lock and identification data within the semaphore is cached in a multiprocessor environment. (Abstract). An arbiter is resource scheduling device that is coupled to the logical plurality of processors (Fig.6, element 506). Semaphore memory holds the semaphore for the entire set of resources (Fig.6, element 504). Spin buffer is a semaphore checker (Fig.6, element 502, spin buffer) that is coupled to arbiter which is a resource scheduling device and the semaphore (semaphore memory). Spin buffer thus provides the information within the semaphore relating to the ownership status of the shared resource. (col.3, lines 3-5). When the logical plurality of processors (fig.5, Bus Masters, 406A, 406B, 406C, and 406D) need access to a shared resource and after they initiate the read for the ownership (requests for semaphore modification), spin buffer detects (receives) the read for ownership from the devices. Spin buffer then identifies the ownership state of a semaphore corresponding to the requests (col. 5, lines 34-39). If the semaphore is owned by another device , the requesting device is denied access to the shared resource

(declining second modification request). If the requested semaphore is not owned by another requesting device, then the requesting device can read the data from the semaphore, which completes the process of acquiring the ownership of the shared resource (transmitting the identified ownership state and allow the first requesting device to access a shared resource) (col.4, lines 3-9) . Bus controller along with Spin buffer also provides an arbiter which determines whose and when to allow the request for resource ownership to succeed based on the priority and availability of a shared resource (Fig. 4, element 402 (Bus Controller), Fig.5, element 506 (Arbiter), col.4, lines 43-56). Although, the reference Derrick teaches that the first modification request is allowed to succeed if the identified ownership state corresponds to no ownership, and indicates that Bus controller (Arbiter) assigns a priority which determines which semaphore modification request is allowed, the reference fails to explicitly teach to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device, however it is well known in the art to implement the desired protocol for the priority determining the order of granting the requests for semaphore modifications such as round robin. Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a means which causes machine to receive the requests for semaphore modifications, to identify an ownership state of a semaphores corresponding to semaphore modification requests, arbitrate and allow the modification requests to succeed as desired, in this case the first modification request to succeed if the identified ownership state corresponds to the first

requesting device. Because, it is economical and efficient to share a resource among multiple processors rather than each processor is having a complete set of resources.

Referring to claim 20,

20. The multiprocessor recited in Claim 17 wherein each of the one or more semaphore modification requests received identify a corresponding requesting processor of the one or more of the logical plurality of processors.

Derrick teaches having a separate identification of each requesting logical processor of the one or more of the logical plurality of processors connected to each port of spin buffer thus Derrick's spin buffer is capable of discriminating between the individual logical processors when it comes to prioritizing the semaphore modification requests. (col.5, lines 53-67 and col.6, lines 1-9).

Referring to claim 21,

21. The multiprocessor recited in Claim 17 wherein the multiprocessor is fabricated on a single die.

Claim 21 is rejected for the reasons set forth in above paragraph for claims 4 and 5.

Referring to claim 24, 25, 26, 27 and 30,

24. An apparatus comprising:

a register to access a shared resource of a set of resources;

a semaphore corresponding to the shared resource; and

a semaphore checker coupled to the semaphore to allow access to the shared resource through the register.

25. The apparatus of Claim 24 wherein the semaphore checker is further to:

receive one or more semaphore modification requests from one or more of a logical plurality of processing devices,

identify an ownership state of the semaphore,

arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting device of the one or more of the logical plurality of processing devices,

allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device; and

allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

26. The apparatus of Claim 25 wherein the semaphore checker is further to:

decline a second modification request of the one or more semaphore modification requests.

27. The apparatus of Claim 25 wherein the semaphore checker is further to:

receive a semaphore read requests from one of the one or more of the logical plurality of processors;

transmit the identified ownership state in response to the semaphore read request; and

allow the first requesting processor to access a shared resource.

30. The apparatus of Claim 25 wherein arbitration is resolved on a round-robin basis.

Derrick teaches the spin buffer where the lock and identification data within the semaphore is cached in a multiprocessor environment. (Abstract). Semaphore memory

holds the semaphore for the entire set of resources (Fig.6, element 504). Spin buffer is a semaphore checker (Fig.6, element 502, spin buffer) that is coupled to arbiter is a resource scheduling device and the semaphore (Fig.6, element 504, semaphore memory). The arbiter is a resource scheduling device that is coupled to the logical plurality of processing devices (Fig.6, element 506). Spin buffer thus provides the information within the semaphore relating to the ownership status of the shared resource. (col.3, lines 3-5). When the logical plurality of processing devices (fig.5, Bus Masters, 406A, 406B, 406C, and 406D) need access to a shared resource and after they initiate the read for the ownership (requests for semaphore modification), spin buffer detects (receives) the read for ownership from the devices. Spin buffer then identifies the ownership state of a semaphore corresponding to the requests (col. 5, lines 34-39). If the semaphore is owned by another device , the requesting device is denied access to the shared resource (declining second modification request). If the requested semaphore is not owned by another requesting device, then the requesting device can read the data from the semaphore, which completes the process of acquiring the ownership of the shared resource (transmitting the identified ownership state and allow the first requesting device to access a shared resource) (col.4, lines 3-9) . Bus controller along with Spin buffer also provides an arbiter which determines whose and when to allow the request for resource ownership to succeed based on the priority and availability of a shared resource (Fig. 4, element 402 (Bus Controller), Fig.5, element 506 (Arbiter), col.4, lines 43-56). Although, the reference Derrick teaches that the first modification request is allowed to succeed if the identified ownership state

corresponds to no ownership, and indicates that Bus controller (Arbiter) assigns a priority which determines which semaphore modification request is allowed, the reference fails to explicitly teach to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device, however it is well known in the art to implement the desired protocol for the priority determining the order of granting the requests for semaphore modifications such as round robin. Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a means which causes machine to receive the requests for semaphore modifications, to identify an ownership state of a semaphores corresponding to semaphore modification requests, arbitrate and allow the modification requests to succeed as desired, in this case the first modification request to succeed if the identified ownership state corresponds to the first requesting device. Because, it is economical and efficient to share a resource among multiple processors rather than each processing device is having a complete set of resources.

Referring to claim 28,

28. The apparatus of Claim 25 wherein each of the one or more semaphore modification requests received identify a corresponding requesting device of the one or more of the logical plurality of processing devices.

Claim 28 is rejected for the reasons set forth in above paragraph for claim 20.

Referring to claim 29,

29.The apparatus of Claim 25 wherein the logical plurality of processing devices are integrated on a single die.

Claim 29 is rejected for the reasons set forth in above paragraph for claims 4 and 5.

Conclusion

Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (571) 272-3972. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A. Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abp
***

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100